CURRENT-MODE BINARY AND TERNARY ELEMENTS

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Keywords: mixed analog-digital system, digital circuit, current-mode gate, current mode logic, ternary logic

Abstract: Current-mode digital circuits operating with constant, continuous power supply current are presented. These gates fulfil demands for low noise digital circuits for mixed analog-digital systems and are useful for binary and ternary logic. SPICE simulations based on extracted parameters from the layout of the introduced gate and from the layout of classical voltage inverter are shown for comparison. The elementary operations, which form current mode gate basis and elementary logical operations in this basis have been described. Based on these expressions, the functional schemes of various one-bit adder sircuits were designed. The obtained circuits are characterized by smaller hardware overhead in comparison with similar ones based on others gate types.

Introduction

There is a tendency to implement small, intelligent electronic equipment in almost every fields of human activity. On the other hand, today's importance of multimedia results yet require realizations of mixed analog-digital systems, leading to implementations of both analog and digital circuits on a common semiconductor substrate. Rapid progress in silicon VLSI technologies has made it possible to implement multi-function and high performance electronic circuits on single die. However switching transients in digital circuits can perturb analog circuits integrated on the same die by means of coupling through the substrate. There are several solutions for substrate interference reduction - the use of physical separation of analog and digital circuits, diffused guard bands, supply filters, and a low-inductance substrate bias. Another - alternative way for minimizing substrate crosstalk, is a design of interference-resistant analog circuits together with low-level interference-generating digital circuits [1, 2, 3, 4, 5], for example on the current mode gates [1]. Due to the nearly constant significance of power supply current at the different gates states, the level of its noise is lower in comparison with other types gates. Therefore in this paper, the problem of designing digital circuits based on the current-mode gates is considered. Note, that the important property of this current-mode gates basis is possibility of the designing and optimizing of logical functions by their representation as algebraic sum of the set of more simple functions which are selected heuristically. It will be shown in the paper, that the use of above mention approach and properties of current-mode basis allows essentially to reduce the complexity of designing circuits. As a result of design, the functional schemes of various one-bit adders were derived. The obtained circuits are characterized up to 20% smaller hardware overhead in comparison with its prototypes based on others type gates.

Low-noise current-mode gate

Fig. 1 represents a concept of an universal, current mode digital circuit [1]. This circuit operates with a continuous, constant current drawn from the power supply and generates low values of current and voltage signals, which fulfil the requirement for minimizing the substrate interferences.
Using a simple saturation-mode transistor model one can write the equation for the output current in the following form:

$$I_o = I_q - K_2\left(\sqrt{\frac{I_i}{K_1}} + V_{T1} - V_{T2} - V\right)^2 \tag{1}$$

$$K_i = \frac{K'}{2}\left(\frac{W_i}{L_i}\right), \quad i = 1,2 \tag{2}$$

where: V_{T1}, V_{T2} - threshold voltages of n-MOS transistors.

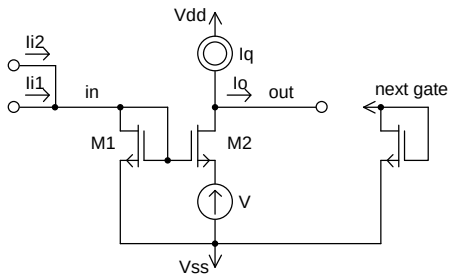


Fig. 1. Concept of current-mode gate

Determinations of levels of a current for logical "0" and logical "1" at the input "in" of the current-mode gate and corresponding logical states at the output "out" are as follows:
Logical "0" at the input corresponds to:

$$I_i \le K_1 \cdot V^2. \tag{3}$$

In this case, the output current *Io = Iq* means the logical "1" at the output "out".
Logical "1" at the input corresponds to:

$$I_i \ge K_1 \cdot \left(V + \sqrt{\frac{I_q}{K_2}}\right)^2. \tag{4}$$

Then the output current *Io = 0* means the logical "0" on the output of the gate.
Therefore, the circuit in Figure 1 performs logical inversion (NOT-operation).
CMOS realization of the concept is shown in Fig. 2(a). For comparison of used techniques - the classical, voltage gate circuit (see Fig. 2(b)) has been also simulated. Layouts of both gates have been designed in a standard 0.8 mm polysilicon-gate and double-metal CMOS technology *cmn8a* from VLSI Technology Inc., and then the circuits have been extracted.

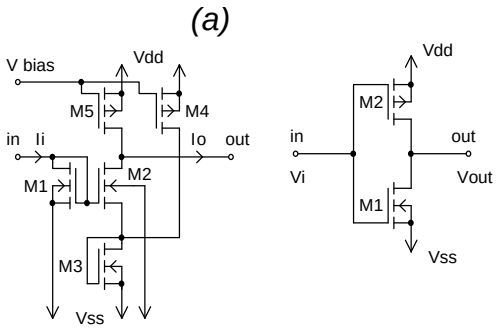


Fig. 2. Current-mode CMOS digital gate (a) and classical, voltage CMOS inverter (b)

Note, that when more than one excitation of value which can fulfil equation (4) is given, then circuit in Fig. 1 performs logical negation of alternative (NOR-operation).

Therefore it is unnecessary to use many different circuits according to the needed number of inputs as it is with voltage gates. In addition, in low-voltage realization of voltage-mode digital circuits, only not more than two-input gates are used. It is known that a number of transistors in the current path influence an ability of operation with low voltages. Presented current gate has three transistors in a current path.

On the other hand voltage technique in digital circuits allows to connect inputs to one output, while in current-mode digital technique many outputs of one gate should be used to assure an independence of nets. The way of connecting additional outputs is presented in Fig. 3.

At a first look, it seems to be a difficulty with a necessity to connect several lines from outputs into the next gate input. It should be remarked that a fact of creation of logical combination in the net of interconnection allows to link gates with well known, minimal total path length routing methods. Instead of that, the main problem is a distribution and routing current mode clock signals in synchronous digital circuits. Thus, for the future, the most promising seems to be pipeline-processing technique and associated with it parallel processing. Today, this concept is even welcomed. Note, that since the speed of processors is being limited more and more by the global signal routing, an architecture which seeks to limit these effects may indeed result in a significant speed increase.

Increasing of number of inputs in voltage technics leads to the increase of number of transistors between VDD and ground in the current path. Such a problem does not appear in the presented approach. Of course, for the great number of gate outputs directed to one input - the voltage VDS=VGS in the input transistor may increase largely disturbing constant value of current drawn from the power supply.

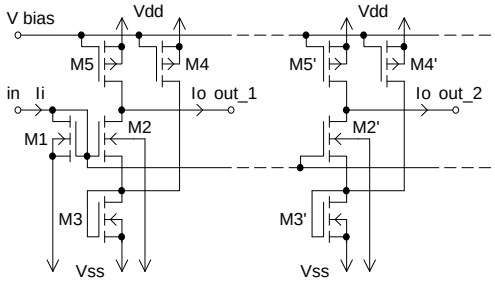


Fig. 3. The way of connecting outputs

Let us consider on operation of the ring oscillator circuit composed of seven gates (Fig. 4).

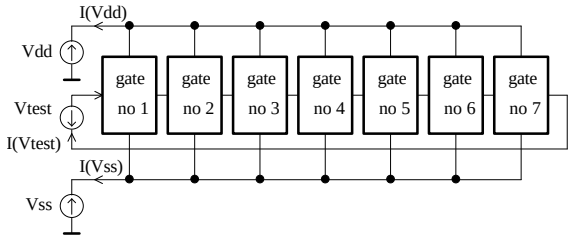
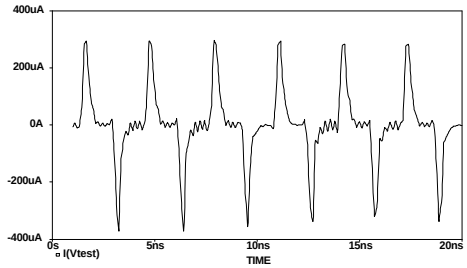


Fig. 4. Ring oscillator composed of seven gates

The current-mode gate shows lower current and voltage swing for taken values of *Iq* though it is slower compared to voltage gate (Fig. 5) for those values.
Note, that in the case of using voltage gates, the power supply current I(VDD) has non-zero value comparable to current I(VDD) drawn by the ring oscillator composed of current-mode gates (see Fig. 6). As one can easily state, in such a case, there is no differences between voltage- and current-mode gates regarding the power consumption.

(a)



(b)

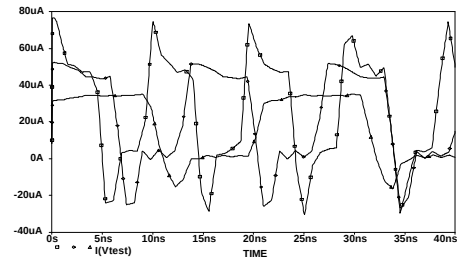
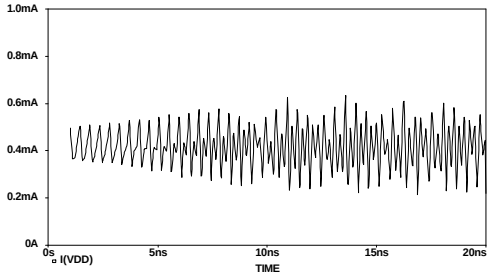


Fig. 5. Current flow through Vtest source:
(a) classical inverters, (b) current-mode gates

(a)



(b)

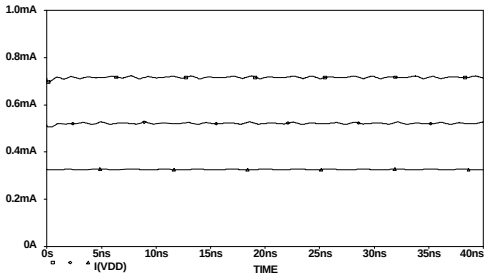


Fig. 6. Supply current I(VDD) feeding oscillator: (a) classical inverters, (b) current-mode gates

BINARY LOGIC WITH CURRENT-MODE GATES

All binary operations can be realized with current-mode gates, but there is no individual gate responsible for performing the function - each operation except an inversion takes place in the connections between the gates. On the other hand less number of fundamental circuits is more suitable for automatic design and manufacturing.

Therefore, in the logic meaning, current-mode inverter is represented by the following equation:

$$\overline{X} = \begin{cases} 1 \text{ if } X \le 0 \\ 0 \text{ if } X > 0 \end{cases} \quad (5)$$

Realizations of three Boolean elementary logical operations are presented below.

Operation $\overline{a}$ (NOT)

Analytic description of this operation in the Boolean basis is represented by expression $\overline{a}$, and analytic description for implementation in the current-mode gates basis is the same. Fig. 7. shows implementation of the NOT operation.

Fig. 7. Boolean symbol of the NOT operation (a) and its current-mode implementation (b)

Operation $a\&b$ (AND)

Analytic description of the AND operation in the Boolean basis is represented by expression:

$$a\&b, \quad (6)$$

while analytic description for implementation in the current-mode gate basis is:

$$\overline{\overline{a}+\overline{b}}. \quad (7)$$

Fig. 8. shows the implementation of the AND operation.

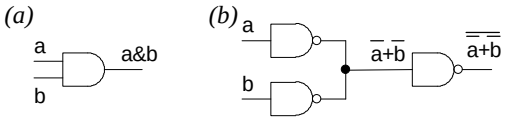


Fig. 8. Boolean symbol of the AND operation (a) and its current-mode implementation (b)

Operation $a \vee b$ (OR)

Analytic description of the OR operation in the Boolean basis is represented by expression:

$$a \vee b, \tag{8}$$

while analytic description for implementation in the current-mode gate basis is:

$$a + b. \tag{9}$$

Fig. 9. shows the implementation of the OR operation.

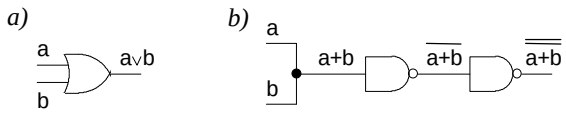


Fig. 9. Boolean symbol of the OR operation (a) and its current-mode implementation (b)

THREE-STATES SYMMETRICAL LOGIC IN THE CURRENT-MODE BASIS. ANTI-INVERTER CIRCUIT

Implementing simple change in the current-mode gate circuit one can achive a brand new gate. The new anti-inverter gate and its symbol are shown in Fig. 10. The circuit from the Fig. 2 without transistor M5 behaves according to following expression:

$$\hat{X} = \begin{cases} 0 \text{ if } X \le 0 \\ -1 \text{ if } X > 0 \end{cases} \tag{10}$$

Fig. 10. Anti-inverter circuit

An extended binary logic can reduce chip area consumption in comparison to ordinary binary logic. We have decided to employ a tri-state logic to save high noise margin. Note that three states, out of the set {-1, 0, 1}, can only appear at the outputs and only the set {0, 1} is received at the input of the gate and is then transformed. In fact all the logical combinations, except an inverting, take place at the interconnections between the gates.

At a first look, it seems to be a difficulty with a necessity to connect several lines from outputs into the next gate input. It should be remarked that a fact of creation of logical combination in the net of interconnection allows to link gates with well known, minimal total path length routing methods. Instead of that, the main problem is a distribution and routing current mode clock signals in synchronous digital circuits. Thus, for the future, the most promising seems to be pipeline-processing technique and associated with it parallel processing. Today, this concept is even welcomed. Note, that since the speed of processors is being limited more and more by the global signal routing, an architecture which seeks to limit these effects may indeed result in a significant speed increase .

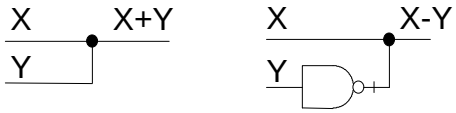
Increasing of number of inputs in voltage technics leads to the increase of number of transistors between V_{DD} and ground in the current path. Such a problem does not appear in the presented approach. Of course, for the great number of gate outputs directed to one input - the voltage $V_{DS}=V_{GS}$ in the input transistor may increase largely disturbing constant value of current drawn from the power supply.

SOME LOGICAL IDENTITIES OF THE CURRENT BASIS AND APPROACH TO MINIMIZATION OF CURRENT-MODE LOGIC FUNCTIONS

Thus, the elementary gates which implement others main logical operations, for example, the operations AND and OR are absent. However, these restrictions of current-mode basis are not shortcomings, because they are compensated by a very easy realization of addition and subtraction operations [2]. For example, an addition operation corresponds, at

the physical level, the addition of currents, each from which represents the value of corresponding operand. In the functional level this means the association of all operand lines into one node. Analogously, a subtraction operation in this approach, at the physical level, is performed by the subtraction of currents. Therefore, in the functional level, this means (for example, for expression *(X-Y)*) the association the line of operand *X* with output of anti-inverter connected to the line of operand *Y*. The example schemes for implementation of operations *(X+Y)* and *(X-Y)* are shown in the fig.11,a and fig.11,b respectively.

It follows from expression (1), (2) and fig.11, that arbitrary logical variable in this basis is (in general case) multivalued one. This means, that appearance of such variable at the any input (output) of the current-mode gate corresponds the appearance at this input (output) the respective level of current in the relative digits [1].



a) *b)*

Fig. 11. The example schemes for realizing addition and subtraction operations in current-mode basis.

Moreover, the significance of variable (or function) appeared on any gate output belongs to the set {-1, 0, 1}, while the significance of variable appeared on any gate input (for example, as a result of addition or subtraction operations) belongs, in general case, to the set of integer numbers from the interval] -∞,∞[. Due to such logical properties, the Boolean algebra identities are not suitable for this basis, however, all Boolean operations can be realized with current-mode gates. Below the expressions for conversion of some Boolean functions into corresponding logical functions of current-mode basis and their transformation are represented.

$$
\begin{aligned}
a \& b &= \overline{\overline{a} + \overline{b}} \\
\overline{a \& b} &= \overline{\overline{\overline{a} + \overline{b}}} \\
a \vee b &= \overline{\overline{a + b}} \\
\overline{a \vee b} &= \overline{a + b} \\
\overline{a} &= \hat{a} + 1 \\
a - b &= a + \hat{b}
\end{aligned}
\qquad (11)
$$

Thus, based on these expressions it is possible to design current-mode digital circuits. In order to this, firstly, it is needed for this circuit to obtain the corresponding logical expressions into Boolean basis, and then by means expressions (11) to implement the transformation of obtained expressions in current-mode ones. Then by means resulting expressions the corresponding circuit may be designed. Note, that the obtained for current-mode expressions are not always effective. In order to reduction of complexity of logical function (mainly, represented by truth table) the approach consisting of its representation as algebraic sum of the set of more simple functions (which are selected heuristically) may be applied.

The correctness of the represented expressions and applying of the proposed approach will be shown below at the examples of one-bit adders synthesis.

DESIGNING OF ONE-BIT ADDERS WITH CURRENT-MODE GATES

One-bit adder is a combinatorial circuit implementing the function of addition of two input operands a_i, b_i and input carry bit c_i . Besides, adder has outputs of sum s_i and output carry bit c_{i+1}. An adder is described by truth table 1 and realizes the following expressions in the Boolean basis:

$$s_i = a_i b_i c_i \vee a_i \overline{b}_i \overline{c}_i \vee \overline{a}_i b_i \overline{c}_i \vee \overline{a}_i \overline{b}_i c_i, \quad (12)$$

and

$$c_{i+1} = a_i b_i \vee a_i c_i \vee b_i c_i \quad (13)$$

Using the expressions (3) - (8), the follows analytical descriptions of these functions in the current-mode gate basis were obtained:

$$s = \overline{\overline{a}_i + b_i + c_i} + \overline{a_i + \overline{b}_i + c_i} + \overline{a_i + b_i + \overline{c}_i} + \overline{\overline{a}_i + \overline{b}_i + \overline{c}_i} \quad (14)$$

$$c_{i+1} = \overline{\overline{a}_i + \overline{b}_i} + \overline{\overline{a}_i + \overline{c}_i} + \overline{\overline{b}_i + \overline{c}_i} \quad (15)$$

The corresponding of expressions (14) and (15) functional scheme of the one-bit adder is represented at Fig. 12.

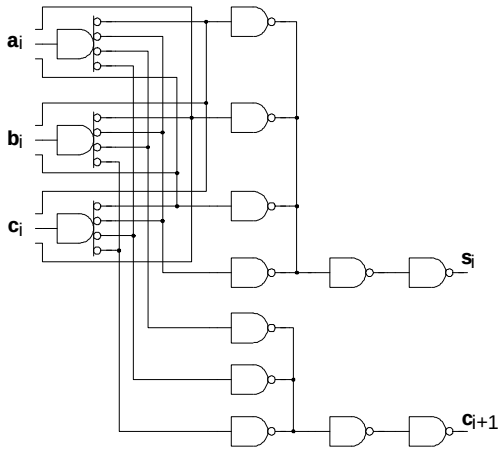


Fig. 12. Example of one-bit adder circuit

Table1. Truth table of the adder in the Boolean basis

c_i	b_i	a_i	$\overline{c}_i$	$\overline{b}_i$	$\overline{a}_i$	c_{i+1}	s_i
0	0	0	1	1	1	0	0
0	0	1	1	1	0	0	1
0	1	0	1	0	1	0	1
0	1	1	1	0	0	1	0
1	0	0	0	1	1	0	1
1	0	1	0	1	0	1	0
1	1	0	0	0	1	1	0
1	1	1	0	0	0	1	1

Note, that obtained scheme of an adder are characterized by many hardware overhead. Therefore, in order to derive the more simple circuit of an adder in the current-mode basis we will use the proposed approach of presentation of functions sum s_i and output carry bit c_{i+1}. as algebraic sum of the set of more simple functions. For example, to the minimization

of function c_{i+1} represented by truth table 1 is possibility its presentation as algebraic sum of the set of next simple functions (see tabl.1):

$$c_{i+1} = \overline{\overline{a_i} + \overline{b_i} + \hat{c}_i}. \qquad (16)$$

Note, that the these functions (named the radix functions) should be always selected by such way, that obtained expression consists smaller operations of inverse or anti-inverse (subtraction).

For the synthesis of the s_i function we have employed analogous approach. As a one of the arguments of algebraic sum the obtained function c_{i+1} was used. Due to this, the following expression for the function s_i was derived:

$$s_i = \overline{c_{i+1}} + \overline{\overline{a_i} + \overline{b_i} + \overline{c_i}} + \overline{a_i \hat{+} b_i + c_i}\,. \qquad (17)$$

The corresponding to expressions (13) and (14) functional scheme of the 10-th gates adder is presented in Fig.13.

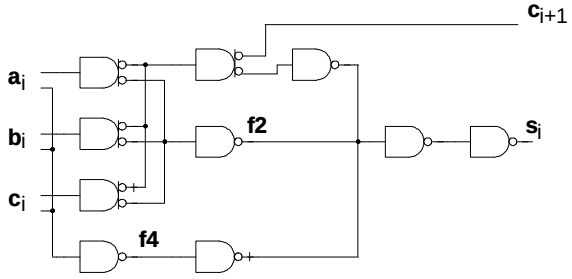


Fig.13. The 10-th gates version of one-bit adder

Table 2 represents the truth table of this adder, where

$$f_1 = \overline{a_i} + \overline{b_i}\,,$$
$$f_2 = \overline{\overline{a_i} + \overline{b_i} + \overline{c_i}}\,,$$
$$f_3 = \overline{\overline{a_i} \hat{+} \overline{b_i} + \overline{c_i}}\,,$$
$$f_4 = \overline{a_i + b_i + c_i}\,.$$

Note that by means expressions (11) and selection the others of radix functions it is possible to derive, for example, the following expressions for function s_i

$$s_i = \overline{\overline{c_{i+1}} + \overline{\overline{a_i} + \overline{b_i} + \overline{c_i}} + \overline{a_i + b_i + c_i}} \qquad (18)$$

and

$$s_i = \overline{c_{i+1} + \overline{\overline{a} \hat{+} \overline{b} + \overline{c}} + \overline{a + b + c}} \qquad (19)$$

These expressions determine (together with expression (16)) the 9-th and 8-th gates versions of one-bit adder correspondingly. They are represented on fig.14 and fig.15.

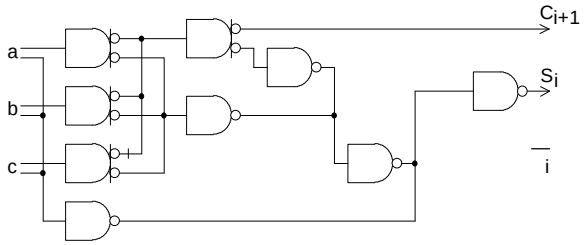


Fig. 14. The 9-th gates version of one-bit adder

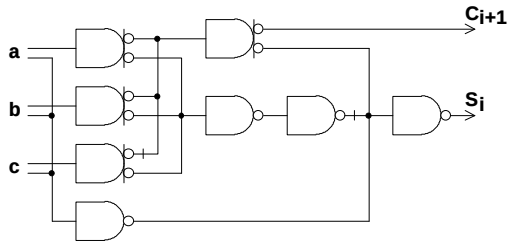


Fig. 15. The 8-th gates version of one-bit adder

Note that last circuit is characterized by following delays and power supply current parameters which were obtained by SPICE simulation of this circuit:

$T(c_{i+1})max = 19.480$ ns

$T(c_{i+1})min = 15.733$ ns

$T(s_i)max = 29.896$ ns

$T(s_i)min = 18.555$ ns

$I_{dd} = 1{,}58$ mA

Thus, the obtained versions of one-bit addersare characterized by smaller hardware overheads in comparison with similar ones based on others gate types.

CONCLUSIONS

The research of problems of the digital circuits designing into current-mode gates basis showed the possibility the realization of the effective mixed analog-digital systems with low level of common noise on a common chip. The logical properties of this gates basis and the proposed several identities for conversion of expressions from Boolean basis is base of the proposed approaches to the design and minimization of digital current-mode circuits and allow to reduce the hardware overheads for circuits realization. As a result, the some functional schemes of one-bit adders were derived. The obtained circuits are characterized by smaller hardware overheads in comparison with similar ones based on others gate types.

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Work supported by the grant KBN 8T11B04214.